**In the Abstract**

**Delete the Abstract it its entirety and replace it with the following Abstract.**

A self-aligned shallow trench isolation region for a memory cell array is formed by etching a plurality of vertical deep trenches in a substrate and coating the trenches with an oxidation barrier layer. The oxidation barrier layer is recessed in portions of the trenches to expose portions of the substrate in the trenches. The exposed portions of the substrate are merged by oxidization into thermal oxide regions to form the self-aligned shallow trench isolation structure which isolates adjacent portions of substrate material. The merged oxide regions are self-aligned as they automatically ~~aligned~~ align to the edges of the deep trenches when merged together to define the location of the isolation region within the memory cell array during IC fabrication. The instant self-aligned shallow trench isolation structure avoids the need for an isolation mask to separate or isolate the plurality of trenches within adjacent active area rows on a single substrate.